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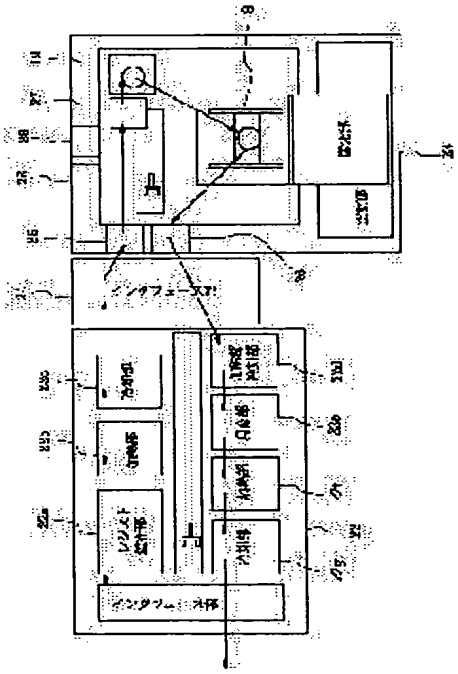
(54) ALIGNER, COATER DEVELOPER, DEVICE MANUFACTURING SYSTEM, DEVICE FABRICATING METHOD, SEMICONDUCTOR PRODUCING FACTORY AND METHOD FOR MAINTAINING ALIGNER

(57)Abstract:
PROBLEM TO BE SOLVED: To carry in/out a wafer without lowering the cleanliness in an aligner and to reduce deterioration of an image performance caused by deterioration of resist.
SOLUTION: A port mechanism for delivering a wafer between a coater developer and an aligner is evacuated and a specified atmospheric gas is introduced. At the time of carrying a wafer into the aligner, the wafer is heated or cooled as required.



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CLAIMS

[Claim(s)]
[Claim 1] The aligner which is an aligner which exposes the pattern of the original edition to a wafer, and is characterized by having the chamber surrounding the predetermined space in this aligner, an air-conditioning machine for adjusting the ambient atmosphere in this aligner, and the port section that has a load lock mechanism.
[Claim 2] Said port section is an aligner according to claim 1 characterized by having the exhauster style which exhausts the gas of these port circles, and the feeder style which supplies gas to these port circles.
[Claim 3] Said port section is an aligner according to claim 1 characterized by having the door which intercepts between the aligner exterior and these port sections, and the door which intercepts between said chamber and these port sections.
[Claim 4] Said port section is an aligner according to claim 1 characterized by preparing more than one.
[Claim 5] Said port section is an aligner according to claim 4 characterized by having the 1st port section for carrying in a wafer, and the 2nd port section for taking out a wafer.
[Claim 6] The aligner according to claim 1 characterized by having the interface section which stocks a wafer between said port sections and said aligner exteriors.
[Claim 7] This interface section is an aligner according to claim 6 characterized by having a load lock mechanism.
[Claim 8] This interface section is an aligner according to claim 6 characterized by being shared between the 1st port section for carrying in a wafer, and the 2nd port section for taking out a wafer.
[Claim 9] This interface section is an aligner according to claim 6 characterized by being prepared between said port section and coat DIBE rope equipment.
[Claim 10] Said port section is an aligner according to claim 1 characterized by having the temperature control device which controls the temperature of said wafer.
[Claim 11] Said temperature control device is an aligner according to claim 10 characterized by having the heater which heats said wafer.
[Claim 12] Said heater is an aligner according to claim 11 characterized by heat-treating a wafer.
[Claim 13] The object of said heat-treatment is an aligner according to claim 12 characterized by being the wafer which applied the resist.
[Claim 14] Said heater is an aligner according to claim 11 characterized by heat-treating the exposed wafer.
[Claim 15] Said temperature control device is an aligner according to claim 10 characterized by having the condensator which cools said wafer.
[Claim 16] Said condensator is an aligner according to claim 15 characterized by cooling the heated wafer.

[Claim 17] The aligner according to claim 10 characterized by performing temperature control of the wafer by said temperature control device while bringing the internal ambient atmosphere of said port section close to the internal ambient atmosphere of said aligner.
[Claim 18] The aligner according to claim 10 characterized by performing temperature control of the wafer by said temperature control device while exhausting the gas of said port section.
[Claim 19] The aligner according to claim 18 characterized by heating said wafer while exhausting the gas

of said port section.
[Claim 20] The aligner according to claim 18 characterized by cooling said wafer while supplying gas to said port section.
[Claim 21] The aligner according to claim 1 characterized by having the temperature selector which controls the temperature of said wafer inside said chamber.
[Claim 22] The aligner according to claim 1 characterized by having the air-conditioning machine which adjusts the perimeter ambient atmosphere of said temperature selector apart from said air-conditioning machine.
[Claim 23] The process which conveys the wafer which applied the resist or the acid-resisting agent to the port section which is the wafer conveyance approach of conveying a wafer in an aligner, and has a load lock mechanism, The wafer conveyance approach characterized by having the process which heats the wafer conveyed by this port section, the process which exhausts the gas of this port section, the process which cools the this heated wafer, the process which supplies gas to this port section, and the process which conveys the wafer of this port section to an aligner.
[Claim 24] The wafer conveyance approach according to claim 23 characterized by having further the process which carries out temperature control of the wafer conveyed by said aligner with the temperature selector inside an aligner.
[Claim 25] The wafer art characterized by having the process which applies a resist or an acid-resisting agent to a wafer, the process which heat-treats this wafer, and the process which exhausts the perimeter ambient atmosphere of a wafer before heat-treatment of a wafer is completed.
[Claim 26] The wafer art according to claim 25 characterized by having the process which supplies gas to the perimeter of this wafer after exhausting the perimeter ambient atmosphere of said wafer.
[Claim 27] The wafer art according to claim 25 characterized by having the process which cools the heated wafer before the process which supplies gas to the perimeter of said wafer is completed.
[Claim 28] Coat DIBE rope equipment which is coat DIBE rope equipment which has the resist spreading section which applies a resist to a wafer, and the development section which develops the exposed wafer, and is characterized by having the door which intercepts between the heating units prepared in the exterior of this coat DIBE rope equipment in order to prebake a wafer.
[Claim 29] Coat DIBE rope equipment according to claim 28 characterized by having a hand for taking out a wafer to said heating unit.
[Claim 30] Coat DIBE rope equipment according to claim 29 characterized by having the control device which controls this hand.
[Claim 31] Said control unit is coat DIBE rope equipment according to claim 30 characterized by choosing two or more external heating units, and controlling conveyance of a wafer.
[Claim 32] Coat DIBE rope equipment according to claim 30 characterized by having further the hand which carries in a wafer from the equipment of the exterior of coat DIBE rope equipment apart from said hand.
[Claim 33] The hand which carries in said wafer is coat DIBE rope equipment according to claim 32 characterized by being the hand which carries in the wafer heated from the equipment of the exterior which heats the wafer after exposure.
[Claim 34] Coat DIBE rope equipment according to claim 28 characterized by having the spreading section of an acid-resisting agent further.
[Claim 35] It is coat DIBE rope equipment according to claim 34 characterized by performing spreading of the acid-resisting agent by said spreading section at least to one side before resist spreading and after resist spreading.
[Claim 36] The device manufacturing system characterized by to have the temperature-control device which is established between the coat DIBE rope equipment which has the resist spreading section which applies a resist to a wafer, and the development section which develops the exposed wafer, the aligner which exposes the pattern of the original edition to a wafer, and this coat DIBE rope equipment and this aligner, is prepared in the port section which has a load lock mechanism, and this port section, and controls the temperature of a wafer.
[Claim 37] Said port section is a device manufacturing system according to claim 36 characterized by having the exhauster style which exhausts the gas of these port circles, and the feeder style which supplies gas to these port circles.

[Claim 38] Said temperature control device is a device manufacturing system according to claim 36 characterized by heat-treating a wafer.
[Claim 39] The object of said heat-treatment is a device manufacturing system according to claim 38 characterized by being the wafer which applied the resist.
[Claim 40] A device manufacturing system given in the claim 36 characterized by having further the control device controlled to perform said heat-treatment while bringing the ambient atmosphere of these port circles close to the internal ambient atmosphere of said aligner, after a wafer is conveyed by said port section.
[Claim 41] The process which is the device manufacture approach and installs the manufacturing installation group for [various] processes in a device manufacturing system in a semi-conductor plant, It has the process which manufactures a semiconductor device by multiple processes using this manufacturing installation group. Said device manufacturing system The coat DIBE rope equipment which has the resist spreading section which applies a resist to a wafer, and the development section which develops the exposed wafer, The device manufacture approach characterized by having the temperature control device which is established between the aligner which exposes the pattern of the original edition to a wafer, and this coat DIBE rope equipment and this aligner, is prepared in the port section which has a load lock mechanism, and this port section, and controls the temperature of a wafer.
[Claim 42] The device manufacture approach according to claim 41 of having further the process which connects said manufacturing installation group in a Local Area Network, and the process which carries out data communication of the information about at least one set of said manufacturing installation group between said Local Area Networks and external networks besides said semi-conductor plant.
[Claim 43] The device approach according to claim 41 characterized by carrying out data communication through said external network between semi-conductor plants other than said semi-conductor plant, and performing production control or it accesses the database which the vendor or user of said aligner offers through said external network and acquires the maintenance information on said manufacturing installation by data communication.
[Claim 44] The manufacturing installation group [in / it is a semi-conductor plant and / a device manufacturing system] for [various] processes, It has the gateway made accessible to the external network outside works from the Local Area Network which connects this manufacturing installation group, and this Local Area Network. It makes it possible to carry out data communication of the information about at least one set of said manufacturing installation group. Said device manufacturing system The coat DIBE rope equipment which has the resist spreading section which applies a resist to a wafer, and the development section which develops the exposed wafer, The semi-conductor plant characterized by having the temperature control device which is established between the aligner which exposes the pattern of the original edition to a wafer, and this coat DIBE rope equipment and this aligner, is prepared in the port section which has a load lock mechanism, and this port section, and controls the temperature of a wafer.
[Claim 45] The process which it is the maintenance procedure of the aligner installed in the semi-conductor plant, and the vendor or user of said aligner provides with the maintenance database connected to the external network of a semi-conductor plant, The process to which access to said maintenance database is permitted through said external network from the inside of said semi-conductor plant, It has the process which transmits the maintenance information accumulated in said maintenance database to a semi-conductor plant side through said external network. Said aligner The maintenance procedure of the aligner characterized by having the chamber surrounding the predetermined space in this aligner, an air-conditioning machine for adjusting the ambient atmosphere in this aligner, and the port section that has a load lock mechanism.
[Claim 46] The aligner characterized by making it possible to be the aligner which exposes the pattern of the original edition to a wafer, to have the chamber surrounding the predetermined space in this aligner, the air-conditioning machine for adjusting the ambient atmosphere in this aligner, the port section that has a load lock mechanism, a display, a network interface, and the computer that performs software for networks, and to carry out data communication of the maintenance information on the aligner concerned through a computer network.
[Claim 47] Said software for networks is an aligner according to claim 46 which makes it possible to offer the user interface for accessing the maintenance database which connects with the external network of

the works in which said aligner was installed, and the vendor or user of said aligner offers on said display, and to acquire information from this database through said external network.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the maintenance procedure of the aligner used for manufacture of a semiconductor device etc., coat DIBE rope equipment, a device manufacturing system, the device manufacture approach, a semi-conductor plant, and an aligner.
[0002]
[Description of the Prior Art] In order that the exposure light of an aligner may raise the resolution of projection optics and may expose a more detailed pattern, it is in the inclination which shortens wavelength. For example, it is common that they use with in-line one, connecting spreading and developing machine, and aligner which are called the coater developer (coat DIBE rope equipment: CDS) for applying a resist to the wafer before exposure and developing the wafer after exposure in exposure of the short wavelength after KrF which is represented by fluorine excimer laser. This is for a resist's deteriorating with ammonia etc. and affecting the image engine performance which can be burned in order to use a resist with low chemistry resistance. Therefore, in-line connection form is adopted for the purpose of shortening the time amount after spreading, and putting on the bottom of the controlled fixed environment.
[0003] The conventional semi-conductor manufacturing system which adopted such in-line connection form as drawing 16 is shown typically.
[0004] The coat DIBE rope equipment which has the coater by which 51 applies a resist to a wafer, and the developer which develops the wafer after exposure in this drawing (CDS), The interface section to which 52 performs an aligner between CDS51 and an aligner 52, and 53 delivers a wafer, The PURIARAIMENTO section for detecting a wafer hand for 54 conveying a wafer to a position and 55, before exposing the reference mark location on a wafer, the wafer stage which 56 carries a wafer and is driven in X, Y, Z, theta, and the direction of a tilt, and 57 are the manual carrying-in taking-out port sections. In order to prevent the poor measurement by telescopic motion of a wafer in the PURIARAIMENTO section 55, PURIARAIMENTO is performed to the wafer of predetermined temperature.

[0005] Next, the flow of an actual wafer is explained using the flow chart of drawing 17 .
[0006] If the wafer which forms a circuit pattern is carried in to CDS51 (step 101), a resist will be first applied to a wafer in resist spreading section 51a of CDS51 (step 102). Then, heating at high temperature (prebaking) is once carried out by heating unit 51b (step 103), it is cooled by cooling section 51c (step 104), and a wafer is **. Then, a wafer is received and passed to an aligner 52 through an interface 53 (step 105) (step 106). The wafer carried in in the aligner 52 is the PURIARAIMENTO section 55, and after PURIARAIMENTO is performed (step 107), it is laid on the wafer stage 56. In the wafer stage section 56 of an aligner 52, the integrated-circuit image with which alignment (step 108) with a reticle was performed, and the wafer was beforehand set to this wafer is exposed (step 109). The wafer which exposure ended is again returned to CDS51 through the interface section 53. This wafer is developed by development section 51e, after carrying out heating at high temperature (postexposure BEKU and Following PEB are called) (step 110) and cooling in a heating unit and 51d of cooling sections of CDS51 (step 111) (step 112). The time amount to an after [this exposure] development also has big effect on the chemical change of a resist. After development, a wafer passes along 51f of heating units, and 51g of

cooling sections, is taken out from coat DIBE rope equipment 22 (step 113), and is transported to other process unit groups etc.
[0007]
[Problem(s) to be Solved by the Invention] Although the wafer is put on the bottom of a pure fixed environment from beginning to end in the above-mentioned process, when put on the bottom of the same environment as development or an applicator especially in CDS, cleanliness falls. Moreover, in order to put on the bottom of the high environment of cleanliness, it must be ready for an appropriate cost rise.
[0008] Furthermore, recently, since it is in the inclination for the chemistry resistance of a resist to decrease, the criteria of cleanliness are also severe.
[0009] The 1st purpose of this invention is to perform carrying-in appearance of a direct wafer from CDS, without solving the technical problem of the above-mentioned conventional technique, and reducing the cleanliness inside an aligner.
[0010] The 2nd purpose of this invention is to reduce degradation of the image engine performance resulting from resist degradation.
[0011]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, it is the aligner of this invention, and the aligner which exposes the pattern of ****** to a wafer, and is characterized by having the chamber surrounding the predetermined space in this aligner, an air-conditioning machine for adjusting the ambient atmosphere in this aligner, and the port section that has a load lock mechanism.
[0012] It is desirable to usually have the exhauster style which exhausts the gas of these port circles, and the feeder style which supplies gas to these port circles in the port section, and to have the door which intercepts between the aligner exterior and these port sections, and the door which intercepts between a chamber and these port sections.
[0013] Moreover, the port section is good also as a configuration which has the 1st port section for more than one being prepared, for example, carrying in a wafer preferably, and the 2nd port section for taking out a wafer.
[0014] Usually, between the port section and coat DIBE rope equipment, it has preferably the interface section which stocks a wafer between the port section and the aligner exterior. As for this interface section, it is desirable to have a load lock mechanism, and it may be shared between the 1st port section for carrying in a wafer, and the 2nd port section for taking out a wafer.
[0015] It is desirable to prepare the temperature control device which especially controls the temperature of a wafer by this invention in the port section, and it is desirable to provide the heater which heats a wafer, and/or the condensator to cool in a temperature control device. This heater performs heat-treatment of a wafer and/or the exposed wafer, and a condensator is for cooling the heated wafer. It is desirable to cool a wafer, while heating a wafer while temperature control, such as heating of the wafer by the temperature control device, can be performed by this while bringing the internal ambient atmosphere of the port section close to the internal ambient atmosphere of an aligner, for example, exhausting the gas of the port section, and supplying gas to the port section.
[0016] Moreover, it is good for the interior of a chamber also as a configuration which has the temperature selector which controls the temperature of a wafer. In this case, apart from an air-conditioning machine, the air-conditioning machine which adjusts the perimeter ambient atmosphere of a temperature selector is usually formed.
[0017] The process which conveys the wafer which applied the resist or the reflective section inhibitor to the port section which the wafer conveyance approach of this invention is an approach of conveying a wafer in the aligner of above-mentioned this invention, and has a load lock mechanism, The process which heats the wafer conveyed by this port section, and the process which exhausts the gas of this port section, It has further the process which is characterized by having the process which cools the heated this wafer, the process which supplies gas to this port section, and the process which conveys the wafer of this port section to an aligner, and carries out temperature control of the wafer conveyed by the aligner with the temperature selector inside an aligner preferably.
[0018] The wafer art of this invention is characterized by having the process which applies a resist or an acid-resisting agent to a wafer, the process which heat-treats the wafer which applied this resist, and the process which exhausts the perimeter ambient atmosphere of a wafer before heat-treatment of a wafer is completed, and preferably, after it exhausts the perimeter ambient atmosphere of a wafer, it has the

process which supplies gas to the perimeter of this wafer. Before the process which supplies gas to the perimeter of a wafer is completed still more preferably, it has the process which cools the heated wafer.
[0019] The coat DIBE rope equipment of this invention is coat DIBE rope equipment which has the resist spreading section which applies a resist to a wafer, and the development section which develops the exposed wafer, and it is characterized by having the door which intercepts between the heating units prepared in the exterior of this coat DIBE rope equipment in order to prebake a wafer.
[0020] This coat DIBE rope equipment has the control unit which usually controls the hand and this hand for taking out a wafer to a heating unit. Two or more external heating units can be chosen, and conveyance of a wafer can be controlled by this control unit. Moreover, the hand which may have further the hand which carries in a wafer from the equipment of the exterior of coat DIBE rope equipment apart from the above-mentioned hand, and carries in a wafer can be used as a hand which carries in the wafer heated from the equipment of the exterior which heats the wafer after exposure.
[0021] The resist spreading section which the device manufacturing system of this invention has the aligner of above-mentioned this invention, and/or coat DIBE rope equipment of above-mentioned this invention, and applies a resist to a wafer, The coat DIBE rope equipment which has the development section which develops the exposed wafer, It is prepared between the aligner which exposes the pattern of the original edition to a wafer, and this coat DIBE rope equipment and this aligner, is prepared in the port section which has a load lock mechanism, and this port section, and is characterized by having the temperature control device which controls the temperature of a wafer.
[0022] The purge gas of a small amount can perform carrying-in taking out of a wafer efficiently, without reducing the cleanliness inside a chamber, when the interior of a chamber is maintained at inert gas ambient atmospheres, such as a predetermined ambient atmosphere, for example, nitrogen, and helium, by the above configuration.
[0023] Moreover, at the time of wafer carrying in to an aligner, since the time amount from heat-treatment to exposure can be shortened, degradation of a resist can be prevented, and at the time of wafer taking out, since heat-treatment can be performed within the ambient atmosphere of the resist spreading section, and the separated exposure ambient atmosphere, resist degradation can be prevented. As a result, degradation of the image engine performance resulting from degradation of a resist is avoidable. When forming a temperature selector in the interior of a chamber, it is desirable to adjust the perimeter ambient atmosphere of a temperature selector with an air-conditioning machine other than the air-conditioning machine for adjusting the internal environment of a chamber. Therefore, the part under the purge environment of an aligner is made into heating of a wafer and the location for cooling, and it considers as temperature control and purge system with an another exposure machine at this part, or the return gas from this part is made into exhaust air or another circulatory system.
[0024] Moreover, since ambient atmosphere permutation in the port section, and heat-treatment (prebaking, PEB) and the continuing cooling processing of a wafer can be performed to coincidence when preparing a temperature control device in port circles, the latency time can utilize effectively and can shorten the time amount from resist spreading to exposure, or the time amount from exposure to development. Consequently, it not only improves a total throughput, but it can reduce degradation of the image engine performance resulting from degradation of a resist.
[0025] Especially, in the 1st port section for wafer carrying in, since the matter of the wafer circumference can be exhausted at the time of heating by controlling under a vacuum (reduced pressure) ambient atmosphere during wafer heating, and applying in the procedure of purging in inert gas at the time of cooling, it becomes possible to be able to reduce the high impurity concentration inside a chamber device, and to attain the high purge engine performance.
[0026] In this invention, if it is not necessary to divide the port section into the object for carrying in and the object for taking out of a wafer and there is one as carrying-in taking-out common use, the above-mentioned purpose can be attained, but in order to arrange in parallel and take two or more wafers in and out, two or more pieces are usually prepared. Moreover, when dividing into the object for carrying in, and taking out and preparing the two port sections, it is good also as a configuration which forms only a wafer heater in the port for wafer taking out.
[0027] Furthermore, it becomes possible to carry out data communication of the maintenance information on an aligner to the aligner of this invention through a computer network by forming a display, a network interface, and the computer that performs software for networks. This software for networks makes it

possible to acquire information from this database through an external network by offering on a display the user interface for accessing the maintenance database which connects with the external network of the works in which the aligner was installed, and the vendor or user of an aligner offers.
[0028] The device manufacture approach of this invention is characterized by having the process which installs the manufacturing installation group containing an aligner and CDS for [various] processes in a semi-conductor plant, and the process which manufactures a semiconductor device by multiple processes using this manufacturing installation group. Furthermore, you may have the process which connects a manufacturing installation group in a Local Area Network, and the process which carries out data communication of the information about at least one set of a manufacturing installation group between a Local Area Network and the external network besides a semi-conductor plant. Moreover, or it accesses the database which the vendor or user of an aligner offers through an external network and acquires the maintenance information on a manufacturing installation by data communication, data communication is carried out through an external network between semi-conductor plants other than a semi-conductor plant, and it may be made to perform a production control.
[0029] The semi-conductor plant of this invention makes it possible to have the gateway made accessible to the external network outside works, and to carry out data communication of the information about at least one set of a manufacturing installation group to it from the Local Area Network which connects the manufacturing installation group and this manufacturing installation group for [containing the aligner and CDS of above-mentioned this invention / various] processes, and this Local Area Network.
[0030] The maintenance procedure of the aligner of this invention is characterized by to have the process which the vendor or user of an aligner provides with the maintenance database connected to the external network of a semi-conductor plant, the process to which access to a maintenance database is permitted through an external network from the inside of a semi-conductor plant, and the process which transmits the maintenance information accumulated in a maintenance database to a semi-conductor plant side through an external network.
[0031]
[Embodiment of the Invention] An example explains this invention below.
[Example 1] drawing 1 is the cross section showing an example of the semi-conductor aligner which makes the light source F2 excimer laser concerning this invention.
[0032] The reticle stage in which 1 carries the reticle by which the pattern was drawn in this drawing, The projection optics to which 2 projects the pattern on a reticle on a wafer, and 3 carry a wafer. X, An illumination-light study system for the wafer stage driven in Y, Z, theta, and the direction of a tilt and 4 to irradiate the illumination light on a reticle, The leading-about optical system to which 5 carries out the light guide of the light from the light source to the illumination-light study system 4, the F2 laser section whose 6 is the light source, The masking blade to which 7 shades exposure light so that it may not be illuminated except the pattern space on a reticle, 8 and 9 respectively the exposure optical axis of reticle stage 1 and wafer stage 3 perimeter A wrap case, helium air-conditioning machine with which 10 adjusts the interior of projection optics 2 and the illumination-light study system 4 in predetermined helium ambient atmosphere, 11 and 12 — cases 8 and 9 — N2 air-conditioning machine which adjusts each interior in N2 predetermined ambient atmosphere — The reticle load lock and wafer load lock which are used when 13 and 14 carry in a reticle and a wafer in a case 8 and 9 respectively, A reticle hand and a wafer hand for 15 and 16 to convey a reticle and a wafer respectively, The reticle alignment mark which uses 17 for the centering control of a reticle, the reticle storage warehouse in which 18 keeps two or more reticles within a case 8, and 19 are the PURIARAIMENTO sections which perform PURIARAIMENTO of a wafer.
[0033] Drawing 2 is the mimetic diagram showing an example of the semi-conductor manufacturing system containing the aligner and coat DIBE rope equipment which were shown in drawing 1 .
[0034] In this drawing, it is the interface section to which the coat DIBE rope equipment (CDS) which has the coater by which 22 applies a resist to a wafer, and the developer which develops the wafer after exposure, and 23 perform an aligner between CDS22 and an aligner 23, and 24 delivers a wafer. Moreover, the in-line port section (25 is the 1st port section and 26 is the 2nd port section), and 28 and 29 are the manual carrying-in taking-out port sections, and 25 and 26 equip every port section with the load lock mechanism. Here, in case a wafer is carried in to an aligner, or in case a load lock mechanism takes out the wafer in an aligner, it intercepts the building envelope of the port section with the exterior, and has a

device for changing the ambient atmosphere inside the port section into the almost same condition as the internal ambient atmosphere of an aligner. In this case, conveyance of a wafer closes a door in order to intercept the building envelope of the port section with outer space, after it changes the internal ambient atmosphere of the exterior and the intercepted port section into the same condition as the internal ambient atmosphere of an aligner, opens the door between the port section and an aligner, and conveys a wafer. In addition, the port section is equipped with the internal ambient atmosphere of an aligner, and the feeder style which supplies the same gas as a load lock mechanism of the port section at the breaker style (for example, door) which intercepts the building envelope of the port section with the exterior, the exhauster style (for example, pump) which exhausts an internal gas in the port section, and the port section. Therefore, the in-line port sections 25 and 26 have N2 gas-supply device, in order to supply the same gas as the door prepared between the interface sections 24, the door prepared between aligners 23, the in-line port section 25 and the exhaust air pump which discharges the gas in 26, and the internal ambient atmosphere of an aligner 23 to the interior. Moreover, the manual carrying-in taking-out port sections 28 and 29 have N2 gas-supply device, in order to supply the same gas as the door prepared between the exteriors, the door prepared between aligners, the manual carrying-in taking-out port section 28 and the exhaust air pump which discharges the gas in 29, and the internal ambient atmosphere of an aligner 23 to the interior. 19 is the PURIARAIMENTO section 19, and it performs PURIARAIMENTO to the wafer of predetermined temperature in order to prevent the poor measurement by telescopic motion of a wafer. 27 is a wafer temperature control part for adjusting a wafer to the above-mentioned predetermined temperature in front of PURIARAIMENTO.

[0035] The above-mentioned interface section 24 may have a load lock mechanism and the same device. That is, in order to change into the same condition as the exhaust air pump which discharges the door by which the interface section 24 was formed between CDS22, the door prepared among the in-line port sections 25 and 26, and the internal gas of the interface section 24 in this case, and the internal ambient atmosphere of the port sections 25 and 26, it has a feeder style for supplying a controlled atmosphere to the interior of the interface section. And in case a wafer is conveyed in the in-line port sections 25 and 26, the internal ambient atmosphere of the interface section 24 is changed into the almost same condition as the building envelope of the in-line port sections 25 and 26. In addition, when giving a load lock mechanism to the interface section 24, the internal ambient atmosphere of the interface section 24 does not need to perform a strict purge like the interior ambient atmosphere of aligner 23, and should just have the capacity of the load lock mechanism of extent put close to the internal ambient atmosphere of the in-line port sections 25 and 26. Thus, contamination of the aligner 23 by the ambient atmosphere of CDS22 or the in-line port sections 25 and 26 can be made to buffer by equipping the interface section 24 with a load lock mechanism. Moreover, the load lock mechanism of the interface section 24 may be made to share between the in-line port section 25 for carrying in a wafer to an aligner 23, and the in-line port section 26 for taking out a wafer from an aligner 23.

[0036] Moreover, you may enable it to stock two or more wafers collectively in the interface section 24.

[0037] Next, the flow of the processing in the semi-conductor manufacturing system of this example shown in drawing 1 and 2 among the wafer processes in semi-conductor manufacture is explained using the flow chart of drawing 3 . In addition, all actuation of each equipment in this example is controlled by the non-illustrated control device, and this control device is controlling the timing of the actuation in a lower flow chart.

[0038] If the wafer which exposes a circuit pattern is carried in to CDS22 (step 201), in resist spreading section 22a of CDS22, a resist will be first applied to a wafer (step 202). Then, a wafer is heated and prebaked in heating unit 22b (100 degrees C, about 1 minute) (step 203), and the wafer heated by cooling section 22c is cooled (step 204).

[0039] The cooled wafer is received and passed to an aligner (step 205) 23 through the interface section 24. The interface section 24 is intercepted from the open air so that the building envelope of CDS22 and the building envelope of an aligner 23 can be connected, via this interface section 24, it is in the open air and the intercepted condition, and a wafer is carried in to the in-line port section 25 which has a load lock function. The in-line port sections 25 and 26 have the door respectively in the CDS22 and aligner 23 side (interface section 24 side). When a wafer is carried in from the interface section 24, the door by the side of an aligner 23 is closed, and if a wafer is carried in, the door by the side of CDS22 is also closed, and it will be in a sealing condition. And with an exhaust air pump, the inside of the in-line port section 25

is decompressed, serves as a vacuum ambient atmosphere, after that, supplies N2 gas to the in-line port section 25, and is made the N2 same ambient atmosphere as the interior of an aligner 23 by N2 gas-supply device (step 206).
[0040] If the inside of the in-line port section 25 reaches a predetermined ambient atmosphere, the door by the side of the aligner 23 of the in-line port section 25 will be opened wide, and a wafer is carried to the wafer temperature control part 27 by the conveyance hand. A wafer is adjusted by predetermined temperature and PURIA rye MENTO is performed in the PURIARAIMENTO section 19 here (step 207). Next, a wafer is laid on the wafer stage 3 and exposure (step 209) of alignment (step 208) with a reticle and an integrated-circuit image is performed.
[0041] Again, since the wafer which exposure ended is returned to CDS22, it is carried in to the in-line port section 26 (step 210). The in-line port section 26 for wafer taking out will be beforehand made N2 ambient atmosphere by the load lock function, by the time exposure processing of step 209 is completed, and even if it opens the door by the side of an aligner 23 wide, it is adjusted so that the ambient atmosphere of the building envelope of an aligner 23 may not be degraded. At first, the door by the side of CDS22 of the in-line port section 26 is closed, carries in a wafer to the in-line port section 26, and closes the door by the side of an aligner 23. Then, the door by the side of an interface 24 is opened wide, and a wafer is passed to CDS22 through the interface section 24.
[0042] Next, a wafer is conveyed by a heating unit and 22d of cooling sections of CDS22, is again heated here for PEB (step 211), and, subsequently is cooled (step 212). And a wafer is conveyed by development section 22e, passes along 22f of heating units, and 22g of cooling sections after development (step 213), is taken out from CDS22 (step 214), and is transported to other process unit groups etc.
[0043] As mentioned above, according to this example, ambient atmosphere degradation inside the equipment when carrying in and taking out a wafer can be prevented to an aligner.
[Example 2] drawing 4 is the mimetic diagram showing an example of the semi-conductor manufacturing system concerning the 2nd example of this invention.
[0044] In this example, heating unit (heater) 32a as a temperature control device of a wafer and cooling section (condensator) 32b are prepared in the 1st in-line port section 32 which delivers the wafer from CDS30 to an aligner 31, and heating unit 33a of a wafer is prepared in the 2nd in-line port section 33 which delivers the wafer from an aligner 31 to CDS30. Therefore, 30f of heating units after resist spreading section 30a, the interface sections 30b and 30c, 30d of cooling sections after PEB, development section 30e, and development and 30g of cooling sections are prepared in CDS30.
[0045] Since the heating unit of PEB is prepared in the heating unit and cooling section list for prebaking at the in-line port sections 32 and 33, to CDS30, it is unnecessary. Moreover, 34 is a wafer temperature control part, and in this example, since temporary temperature control is completed by cooling section 32b, it has only the function to fine-adjust temperature of a wafer.
[0046] In this example, since a bad influence may appear in the definition ability of a resist if PEB is completely performed in a dry environment, in order not to degrade the ambient atmosphere in the case of the aligner 31 at the time of the environmental ambient atmosphere control at the time of PEB, and conveyance of a wafer, it is desirable to prepare a humidity control function in heating unit 33a which performs PEB.
[0047] Next, the structure inside [in-line port section 32] this example is explained to a detail using drawing 5 .
[0048] Drawing 5 is the AA' cross section of the in-line port section 32 of drawing 4 . In this drawing, 42 is a wafer to convey. A supply pipe for 43 to supply N2 which is inert gas to the in-line port section 32, and 44 are the exhaust pipes for making in-line port circles into a vacuum or a reduced pressure ambient atmosphere. When it is the door by which 45a was prepared in the CDS30 side of the in-line port section 32, and the door by which 45b was prepared in the aligner 31 side of the in-line port section 32 and these doors have closed, the in-line port section is sealed. A cooling plate for 46 to cool a wafer 42 and 47 are Peltier devices. A hot plate for 48 to heat a wafer 42 and 49 are heaters. 50 is a wafer hand for conveying a wafer 42 within the in-line port section 32.
[0049] In the semi-conductor manufacturing system of this example, when the wafer 42 to which the resist was applied in resist spreading section 30a is carried in to an aligner 31 from interface 30b, door 45b by the side of the aligner 31 of the in-line port section 32 has closed, and if a wafer 42 is carried in on a hot plate 48, door 45a by the side of CDS30 of the in-line port section 32 will also be closed. Next,

the interior is decompressed by inhalation of air with the exhaust air pump from an exhaust pipe 44, and it considers as a vacuum ambient atmosphere. While decompressing the interior of this in-line port section 32, a hot plate 48 is heated at a heater 49, and prebaking of a wafer 42 is performed. If prebaking of a wafer 42 is completed, a wafer 42 will be moved on the cooling plate 46 by UEHANDO 50. And the wafer 42 on the cooling plate 46 is cooled by Peltier device 47. Moreover, if the internal ambient atmosphere of the in-line port section 32 turns into a desired vacuum ambient atmosphere, N2 gas will be supplied from a supply pipe 43, and the internal ambient atmosphere of the in-line port section 32 is made into the N2 same ambient atmosphere as the interior of an aligner 31. If cooling of a wafer 42 is completed and the inside of the in-line port section 32 reaches N2 predetermined ambient atmosphere, door 45b by the side of the aligner 31 of the in-line port section will be opened wide, and a wafer 42 will be carried to the wafer temperature control part 34 by the conveyance hand 50 of an aligner 31.

[0050] The wafer 42 conveyed by the wafer temperature control part 34 has temperature tuned finely, it is the PURIARAIMENTO section 19 and PURIARAIMENTO is performed. And if the alignment of a wafer 42 and exposure are completed, it will be shortly conveyed by the 2nd in-line port section 33, and PEB is performed by heating unit 33a in this.

[0051] The door (un-illustrating) prepared in the aligner side almost like the 1st above-mentioned in-line port section 32 in order to seal the in-line port section 33, and the door prepared in the CDS30 side are prepared in the 2nd in-line port section 33.

[0052] In the 2nd in-line port section 33, since the reduced pressure and the purge in a port need to be completed before a wafer 42 is carried in, the case of the 1st in-line port section 32 does not need standby of long duration after carrying in a wafer 42 to the 2nd in-line port section 33 from an aligner 31 until it conveys a wafer 42 to interface section 30c. Therefore, it is supposed that only heating unit 33a will be prepared at the 2nd in-line port section 33, without preparing the cooling section.

[0053] In addition, the configuration of this invention is not restricted to the above-mentioned configuration. For example, interface section 30b may be equipped with a load lock mechanism which was stated in the 1st example. Moreover, the 1st heating unit of the in-line port section 32 and cooling section may be separated and constituted. Moreover, in this example, although the 2nd in-line port section 33 is equipped only with heating unit 33a, it may prepare 30d of cooling sections in the 2nd in-line port section 33.

[0054] Moreover, in the above-mentioned explanation, while the heating unit 32 of the 1st in-line port section 32 heated the wafer, the internal ambient atmosphere of the in-line port section 32 was exhausted, while cooling section 32b cooled the wafer, N2 was supplied and the interior of the in-line port section 32 was brought close to the internal ambient atmosphere of an aligner 31. However, this invention is not restricted to this. For example, when taking the time amount which heats a wafer, or when taking the supply time amount of N2, N2 after the exhaust air to the in-line port section 32 may be supplied during heating of a wafer. When similarly taking the time amount which cools a wafer, or when exhaust air of the in-line port section 32 takes time amount, exhaust air of the in-line port section 32 may be continued also during cooling of a wafer. It is desirable to have started exhaust air for the internal ambient atmosphere of the in-line port section 32, before heat-treatment of a wafer is completed at least in the case of which, and before the door by the side of the aligner 31 of the in-line port section opens at least (namely, before the gas supply to the in-line port section is completed), it is desirable to have completed cooling processing of a wafer.

[0055] As mentioned above, according to this example, ambient atmosphere degradation inside the equipment when carrying in and taking out a wafer can be prevented to an aligner, without reducing a throughput.

[0056] Moreover, since according to this example the ambient atmosphere which a wafer sets in an early phase as compared with the former is controlled after applying a resist to a wafer, degradation of the image engine performance resulting from degradation of a resist can be reduced.

[0057] Moreover, since PEB of the wafer exposed in the location by which the ambient atmosphere is controlled is performed according to this example, degradation of the image engine performance resulting from degradation of a resist can be reduced.

[Example 3] drawing 6 is the mimetic diagram showing an example of the semi-conductor manufacturing system concerning the 3rd example of this invention.

[0058] In this example, the heating cooling sections 37a and 38a of a wafer are formed in the in-line port

section 37 which delivers the wafer from CDS35 to an aligner 36, and 38. Therefore, although resist spreading section 35a, development section 35b, and heating cooling section 35c after development are prepared in CDS35, the heating unit and the cooling section of PEB are unnecessary in the heating unit and cooling section list for prebaking. Moreover, the conveyance hand 60 for the in-line port sections 37 and 38 choosing the wafer which applied the resist in resist spreading section 35a either, and conveying it is formed in CDS35.

[0059] Moreover, 34 is a wafer temperature control part, and in this example, since temporary temperature control is completed by heating cooling section 37a, it has only the function to fine-adjust temperature. About other configurations and system configurations of an aligner, it is the same as that of an example 1 or an example 2 fundamentally.

[0060] Next, the flow of the processing in the semi-conductor manufacturing system of this example shown in drawing 6 among the wafer processes in semiconductor device manufacture is explained using the flow chart of drawing 7 . In addition, all actuation of each equipment in this example is controlled by the non-illustrated control device, and this control device is controlling the timing of the actuation in a lower flow chart.

[0061] If the wafer which exposes a circuit pattern is carried in to CDS35 (step 401), in resist spreading section 35a of CDS35, a resist will be first applied to a wafer (step 402). It is carried in to the in-line (step 403) port section 37 through a buffer (un-illustrating) after that. The door by the side of an aligner 36 has closed the in-line port section 37, after a wafer is carried in from the door by the side of CDS35 and being laid on heating cooling section 37a, both doors are closed and it is sealed in the beginning. Next, parallel processing of prebaking (100 degrees C, about 1 minute) and cooling of a wafer is carried out to vacuation of an internal ambient atmosphere, and the supply list of N2 gas (step 404). If the parallel processing in step 404 is completed, the door by the side of an aligner 36 will be opened wide, and a wafer will be carried to the wafer temperature control part 34 by the conveyance hand 60 of an aligner 36. Fine adjustment of temperature is performed so that a wafer may become predetermined temperature, it is the PURIARAIMENTO section 19 and PURIARAIMENTO is performed here (step 405). Next, a wafer is laid on the wafer stage 3 and exposure (step 407) of alignment (step 406) with a reticle and an integrated-circuit image is performed. Since the wafer which exposure ended is again returned to CDS35, it is again carried in to the in-line port section 37 (step 408). The in-line port section 37 has been N2 ambient atmosphere beforehand by the parallel processing of step 404, and even if it opens the door by the side of an aligner 36 wide, it does not degrade the ambient atmosphere of the building envelope of an aligner 36. At the time of this re-carrying in, the door by the side of CDS35 of the in-line port section 37 is closed, and a wafer is laid on heating cooling section 37a of the in-line port section 37. Then, although both doors are closed and sealed and only the door by the side of CDS35 is opened wide, PEB and cooling processing are performed to a wafer also in the meantime in parallel (step 408). And a wafer is passed to CDS35 through a buffer. Next, a wafer is conveyed by development section 35b of CDS35, passes along heating cooling section 35c after development (step 409), is taken out from CDS35 (step 410), and is transported to other process unit groups etc.

[0062] In processing of the above-mentioned wafer, although the in-line port section 38 which built in heating cooling section 38a was not used, the port here is used, when processing two or more wafers continuously. That is, while exposing to the wafer, since the port 37 is left with the internal ambient atmosphere of an aligner 36, it is not applicable to carrying in of the following wafer. Therefore, since carrying-in processing of a wafer can be shortly performed in parallel using the in-line port section 38, it becomes possible to process continuously two or more wafers [be / no latency time]. In addition, the conveyance hand 60 performs supply of the wafer to the in-line port sections 37 or 38, and recovery of the wafer from the in-line port sections 37 or 38 based on the signal from a non-illustrated control unit.

[0063] In addition, according to this example, although the number of the in-line port sections is two, it is not restricted to this. For example, the three or more in-line port sections may be prepared.

[0064] Moreover, according to this example, although the hand 60 prepared in CDS35 is one, it is not restricted to this. For example, two or more hands which convey a wafer alternatively may be prepared in two or more in-line port sections. moreover, the hand for taking out which takes out a wafer alternatively in two or more in-line port sections from the resist spreading section and the hand for carrying in which carries in to the development section the wafer PEB(ed) in the selected in-line port section — ** — it carries out, an application is divided and you may make it form two or more conveyance hands 60

[0065] As mentioned above, according to this example, ambient atmosphere degradation inside the equipment when carrying in and taking out a wafer can be prevented to an aligner, without reducing a throughput.
[0066] Moreover, since according to this example the ambient atmosphere which a wafer sets in an early phase as compared with the former is controlled after applying a resist to a wafer, degradation of the image engine performance resulting from degradation of a resist can be reduced.
[0067] Moreover, since PEB of the wafer exposed in the location by which the ambient atmosphere is controlled is performed according to this example, degradation of the image engine performance resulting from degradation of a resist can be reduced.
[Example 1 of amelioration] drawing 8 is the mimetic diagram of the example of amelioration of the example of above-mentioned drawing 2 . In CDS22, this example is the point of having the spreading section, the heating unit, and the cooling section (22-3 a-c) of the process (TARC:Top Anti-reflective Coating) sake which forms an antireflection film in the upper layer of the spreading section, the heating unit and the cooling section (22-2 a-c) for the process (BARC:Bottom Anti-reflective Coating) which forms an antireflection film in the lower layer of the resist layer in an exposed substrate, and a resist layer, and differs from the example of drawing 2 . Moreover, drawing 9 is the flow chart of the flow of the processing in the semi-conductor manufacturing system of drawing 8 . This example is the point of having the spreading process, heating process, and cooling process (step 204-2 to 204-4) for the spreading process, heating process and cooling process for BARC (step 201-2 to 201-4), and TARC, and differs from the example of drawing 3 .
[0068] In the above-mentioned example, it was only performing spreading of a resist etc. within CDS22. However, there may be BARC and TARC.
[0069] In BARC, the spin coat of the acid-resisting agent is carried out to a wafer like the case where a resist is applied, before resist spreading. Then, heating and cooling are performed for the wafer which coated the acid-resisting agent if needed, and a resist is applied to a wafer. By BARC, reflection of the exposure light from a wafer substrate can be prevented, and the configuration of a resist image can be improved.
[0070] In TARC, the spin coat of the acid-resisting agent is similarly carried out after resist spreading. There may be a process which heats and cools the wafer which coated the resist between TARC(s) the resist spreading back. Heating and cooling are performed for the wafer which coated the acid-resisting agent after TARC if needed. By TARC, improvement in a configuration of the resist image by acid resisting of exposure light can be aimed at, and the electric shielding nature of a resist and an environment can be raised, and configuration degradation of the resist image by the environmental factor can also be prevented.
[Example 2 of amelioration] drawing 10 is the mimetic diagram of the example of amelioration at the time of constituting BARC and resist spreading section 22a-1 which shared BARC spreading section 22-2a of drawing 8 with resist spreading section 22a. In this case, the heating unit and the cooling section for BARC in the above-mentioned example 1 of amelioration (22-2b, 22-2c) can also be shared.
[0071] Similarly, drawing 11 is the mimetic diagram of the example of amelioration at the time of constituting the resist and TARC spreading section 22a-2 which shared TARC spreading section 22-3a of drawing 8 with resist spreading section 22a. In this case, the heating unit and the cooling section for TARC in the above-mentioned example 1 of amelioration (22-3b, 22-3c) can also be shared.
[0072] In this example of amelioration, since spreading of BARC or TARC etc. can be shared with spreading of a resist etc., the simplification and the improvement in a throughput in equipment can be aimed at.
[0073] In addition, it is not necessary to necessarily share the BARC spreading section, the resist spreading section or the resist spreading section, and the TARC spreading section. However, subsequent heating unit and cooling section can be shared.
The heating unit and the cooling section after the [example of amelioration] 3 TARC are not necessarily required.
[0074] Drawing 12 is a mimetic diagram in case there are not a heating process and a cooling process after TARC spreading.
[0075] In this example of amelioration, since heating and cooling after TARC spreading are omissible, the simplification and the improvement in a throughput in equipment can be aimed at.

[Example 4 of amelioration] In the above-mentioned example of drawing 4 -7, heating and cooling were performed in the load lock. It cannot be overemphasized that it may be a process containing above BARC and TARC, or heating and cooling after resist spreading may be performed within a load lock.
[Example 4] drawing 13 is the mimetic diagram showing an example of the semi-conductor manufacturing system concerning the 4th example of this invention.
[0076] Consider only as a load lock function, and the heating cooling sections 41a and 41b as a temperature selector of a wafer are formed in the aligner 39 port section 40a and near the 40b, and also the in-line port sections 40a and 40b to which the semi-conductor manufacturing system of this example delivers the wafer to an aligner 39 are the same as that of an example 3. The heating cooling sections 41a and 41b are being made into circulatory system with the another return gas from this part also under the purge environment of an aligner 39. In addition, it is good also as a configuration which makes the heating cooling sections 41a and 41b temperature control and purge system with an another aligner 39, or exhausts return gas. For this reason, it has the air-conditioning machine which is not illustrated [which adjusts the ambient atmosphere of the perimeter of a temperature selector apart from the air-conditioning machine (un-illustrating) of a purge environment].
[0077] The flow of the processing in the semi-conductor manufacturing system of this example shown in drawing 13 among the wafer processes in manufacture of a semiconductor device is explained using the flow chart of drawing 14 . In addition, all actuation of each equipment in this example is controlled by the non-illustrated control device, and this control device is controlling the timing of the actuation in a lower flow chart.
[0078] In this example, processing of (step 303) is the same as that of an example 3 to wafer carrying in to in-line port section 40a from wafer carrying in (step 301) to CDS35.
[0079] In in-line port section 40a, the door by the side of an aligner 39 has closed, and after a wafer is carried in from the door by the side of CDS35, both doors are closed and sealed in the beginning. Next, vacuum abandonment of the internal ambient atmosphere of in-line port section 40a is once carried out, and N2 gas is supplied to in-line port section 40a after that (step 304). After this processing finishes, the door by the side of an aligner 36 is opened wide, and a wafer is carried to heating cooling section 41a by the conveyance hand of an aligner 39. It prebakes and (step 305) processes [cooling] (step 306), and the wafer laid on heating cooling section 41a is carried to the wafer temperature control part 34 by the conveyance hand of an aligner 36. And PURIARAIMENTO (step 307), alignment (step 308), and exposure (step 309) are performed like an example 3.
[0080] The wafer which exposure ended is again returned to heating cooling section 41a, and PEB(ing) (step 310) and cooling processing are carried out (step 311). And it is again carried in to in-line port section 40a. After in-line port section 40a's having been N2 ambient atmosphere beforehand, having closed the door by the side of CDS35 of in-line port section 40a and carrying in a wafer to in-line port section 40a, both doors are closed and sealed, only the door by the side of CDS35 is opened wide, and a wafer is passed to CDS35 through a buffer (step 312). A wafer is conveyed by development section 35b of CDS35, passes along heating cooling section 35c after development (step 313), is taken out from CDS35 (step 314), and is transported to other process unit groups etc.
[0081] In this example, although explanation of in-line port section 40b and heating cooling section 41b was not given, when processing two or more wafers continuously, it is used like an example 3.
[0082] As mentioned above, according to this example, ambient atmosphere degradation inside the equipment when carrying in and taking out a wafer can be prevented to an aligner, without reducing a throughput.
[0083] Moreover, since according to this example the ambient atmosphere which a wafer sets in an early phase as compared with the former is controlled after applying a resist to a wafer, degradation of the image engine performance resulting from degradation of a resist can be reduced.
[0084] Moreover, since PEB of the wafer exposed in the location by which the ambient atmosphere is controlled is performed according to this example, degradation of the image engine performance resulting from degradation of a resist can be reduced.
[Example 5] drawing 15 is the cross section showing other examples of the semi-conductor aligner which makes the light source F2 excimer laser concerning this invention.
[0085] The whole aligner is covered with the case 20 and, as for the equipment of this example, O2 and H2O of the interior are purged by N2 gas. 21 is an air-conditioning machine for making the case 20 whole

into N2 ambient atmosphere. In this example, it is respectively isolated with the building envelope (drive-system space) of a case 20, and the building envelope of a lens-barrel 2 and the illumination-light study system 4 is independently adjusted by helium ambient atmosphere.
[0086] Although the control approach of the wafer load lock 14 in this example, i.e., the carrying-in attitude method of a wafer, is the same as that of examples 1-4, when the whole equipment does not necessarily need to be purged strictly, it can consider as a simple and cheap equipment configuration (when injecting purge gas near an exposure optical axis etc.).
[0087] According to the configuration explained above, internal environment degradation by the concentration rise of degradation of cleanliness in the aligner at the time of carrying-in appearance, such as a wafer and a reticle, and O2, the amount of H2O, etc. can be prevented. As a result, the operation cost of an air-conditioning machine and the cost of purge gas in an aligner can be held down.
[The example of the system corresponding to a network], next the example of the production system of semiconductor devices (semiconductor chips, such as IC and LSI, a liquid crystal panel, CCD, the thin film magnetic head, micro machine, etc.) are explained. This performs maintenance service, such as trouble correspondence of the manufacturing installation installed in the semi-conductor plant, and a periodic maintenance or software offer, using the computer network besides a plant.
[0088] Drawing 18 cuts down and expresses a whole system from a certain include angle. 101 are the place of business of the vendor (equipment supply manufacturer) which offers the manufacturing installation of a semiconductor device among drawing. As an example of a manufacturing installation, the semiconductor fabrication machines and equipment for [various] processes (assembly equipment, test equipment, etc.) used by the semi-conductor plant, for example, the devices for last processes (lithography equipments, such as an aligner, a photo lithography processor, and an etching system, a thermal treatment equipment, membrane formation equipment, flattening equipment, etc.) and the devices for back processes, are assumed. In a place of business 101, it has the host managerial system 108 which offers the maintenance database of a manufacturing installation, two or more actuation terminal computers 110, and Local Area Network (LAN) 109 which connects these and builds intranet. The host managerial system 108 is equipped with the security function to restrict the gateway for connecting LAN109 to the Internet 105 which is the external network of a place of business, and access from the outside.
[0089] On the other hand, 102-104 are the plants of the semi-conductor manufacture manufacturer as a user of a manufacturing installation. Plants 102-104 may be the works belonging to a mutually different manufacturer, and may be the works (for example, works for last processes, works for back processes, etc.) belonging to the same manufacturer. In each works 102-104, the host managerial system 107 is formed as two or more manufacturing installations 106, Local Area Network (LAN) 111 which connects them and builds intranet, and supervisory equipment which supervises the operation situation of each manufacturing installation 106, respectively. The host managerial system 107 formed in each works 102-104 is equipped with the gateway for connecting LAN111 in each works to the Internet 105 which is the external network of works. Access becomes possible from LAN111 of each works through the Internet 105 at the host managerial system 108 by the side of a vendor 101 by this, and access is [the user restricted by the security function of the host managerial system 108] permitted. The status information (for example, symptom of the manufacturing installation which the trouble generated) which shows the operation situation of each manufacturing installation 106 is specifically notified to a vendor side from a works side through the Internet 105, and also maintenance information, such as a response indication (for example, information, software and data for management which direct the solution for a trouble) corresponding to the notice, and the newest software, help information, is receivable from a vendor side. The communications protocol (TCP/IP) currently generally used by the Internet is used for the data communication between each works 102-104 and a vendor 101, and the data communication in LAN111 in each works. In addition, the high dedicated line networks (ISDN etc.) of security can also be used instead of using the Internet as an external network outside works, without the ability performing access from a third person. Moreover, what [not only] a vendor offers but a user builds a database, a host managerial system places it on an external network, and you may make it permit access to this database from two or more works of a user.
[0090] Now, drawing 19 is the conceptual diagram which cut down and expressed this whole operation gestalt system from the include angle different from drawing 18 . In the previous example, each was what

connects two or more user works equipped with the manufacturing installation, and the managerial system of the vendor of this manufacturing installation in an external network, and carries out data communication of the production control of each works, or the information on at least one set of a manufacturing installation through this external network. On the other hand, this example connects works equipped with the manufacturing installation of two or more vendors, and the managerial system of each vendor of two or more of these manufacturing installations in the external network outside works, and carries out data communication of the maintenance information on each manufacturing installation. Among drawing, 201 are a manufacturing installation user's (semiconductor device manufacture manufacturer) plant, and the aligner 202, the photo lithography processor 203, and the membrane formation processor 204 are introduced into the production line of works as an example the manufacturing installation which performs various processes, and here. In addition, in drawing 19 , although only one plant 201 is drawn, two or more works are similarly connected by network in practice. It connects by LAN206, each equipment in works constitutes intranet, and operation management of a production line is carried out with the host managerial system 205. On the other hand, each place of business of vendors (equipment supply manufacturer), such as the aligner manufacturer 210, the photo lithography processor manufacturer 220, and the membrane formation equipment manufacturer 230, is equipped with the host managerial system 211,221,231 for performing control maintenance of the device supplied, respectively, and these equip it with the gateway of a maintenance database and an external network, as mentioned above. The host managerial system 205 which manages each equipment in a user's plant, and the managerial system 211,221,231 of the vendor of each equipment are connected by the Internet or the dedicated line network which is the external network 200. In this system, although operation of a production line will stop if a trouble occurs in one of a series of manufacture devices of a production line, a prompt action is possible by receiving the control maintenance through the Internet 200 from the vendor of the device by which the trouble occurred, and a pause of a production line can be suppressed to the minimum.

[0091] Each manufacturing installation installed in the semi-conductor plant is equipped with the computer which performs a display, a network interface, software for network access stored in storage, and software for equipment actuation, respectively. As a store, they are an internal memory, a hard disk or a network file server, etc. The above-mentioned software for network access offers the user interface of a screen as shows an example to drawing 20 on a display, including dedication or a general-purpose web browser. The operator who manages a manufacturing installation at each works inputs information, such as the model (401) of manufacturing installation, a serial number (402), the subject name (403) of a trouble, a generating day (404), an urgency (405), a symptom (406), the coping-with method (407), and progress (408), into the input item on a screen, referring to a screen. It is transmitted to a maintenance database through the Internet, and the suitable maintenance information on the result is answered from a maintenance database, and the inputted information is shown on a display. Moreover, the user interface which a web browser offers can pull out further the actuation guide (help information) with which a hyperlink function (410-412) is realized, and the software of the latest version used for a manufacturing installation from the software library which a vendor offers is pulled out, or reference of the operator of works is presented like illustration. [that an operator accesses the still more detailed information on each item]

[0092] Next, the manufacture process of a semiconductor device of having used the production system which gave [above-mentioned] explanation is explained. Drawing 21 shows the flow of the overall manufacture process of a semiconductor device. The circuit design of a semiconductor device is performed at step 1 (circuit design). The mask in which the designed circuit pattern was formed is manufactured at step 2 (mask manufacture). On the other hand, at step 3 (wafer manufacture), a wafer is manufactured using ingredients, such as silicon. Step 4 (wafer process) is called a last process, and forms an actual circuit on a wafer with a lithography technique using the mask and wafer which carried out [above-mentioned] preparation. The following step 5 (assembly) is called a back process, is a process semiconductor-chip-ized using the wafer produced by step 4, and includes assembly processes, such as an assembly process (dicing, bonding) and a packaging process (chip enclosure). At step 6 (inspection), the check test of the semiconductor device produced at step 5 of operation, an endurance test, etc. are inspected. A semiconductor device is completed through such a process and this is shipped (step 7). A last process and a back process are performed at another works of dedication, respectively, and

maintenance is made by the control maintenance system which gave [above-mentioned] explanation for every works of these. Moreover, also between last process works and back process works, data communication of the information for production control or equipment maintenance is carried out through the Internet or a dedicated line network.

[0093] Drawing 22 shows the detailed flow of the above-mentioned wafer process. The front face of a wafer is oxidized at step 11 (oxidation). At step 12 (CVD), an insulator layer is formed on a wafer front face. At step 13 (electrode formation), an electrode is formed by vacuum evaporationo on a wafer. Ion is driven into a wafer at step 14 (ion implantation). A sensitization agent is applied to a wafer at step 15 (resist processing). At step 16 (exposure), printing exposure of the circuit pattern of a mask is carried out at a wafer with the aligner which gave [above-mentioned] explanation. The exposed wafer is developed at step 17 (development). At step 18 (etching), parts other than the developed resist image are shaved off. The resist which etching could be managed with step 19 (resist exfoliation), and became unnecessary is removed. By carrying out by repeating these steps, a circuit pattern is formed on a wafer multiplex. Even if a trouble occurs, quick restoration can be possible for it, and the manufacture device used at each process can raise the productivity of a semiconductor device compared with the former while it prevents a trouble, since maintenance is made by the control maintenance system which gave [above-mentioned] explanation.

[0094]

[Effect of the Invention] Ambient atmosphere degradation inside the equipment when carrying in and taking out a wafer can be prevented to an aligner, without reducing a throughput according to this invention, as explained above.

[0095] Furthermore, according to this invention, the image engine-performance amelioration by prevention of chemistry degradation of a resist and improvement in a total throughput are attained by utilizing effectively the latency time at the time of the carrying-in appearance of a wafer.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the cross section showing an example of the semi-conductor aligner which makes the light source F2 excimer laser concerning this invention.
[Drawing 2] It is the mimetic diagram showing the semi-conductor manufacturing system concerning the 2nd example of this invention.
[Drawing 3] It is the flow chart which shows the flow of the processing in the semi-conductor manufacturing system of drawing 2 .
[Drawing 4] It is the mimetic diagram showing the semi-conductor manufacturing system concerning the 2nd example of this invention.
[Drawing 5] It is the AA' cross section of the in-line port section of drawing 4 .
[Drawing 6] It is the mimetic diagram showing the semi-conductor manufacturing system concerning the 3rd example of this invention.
[Drawing 7] It is the flow chart which shows the flow of the processing in the semi-conductor manufacturing system of this example shown in drawing 6 .
[Drawing 8] It is the mimetic diagram showing the semi-conductor manufacturing system concerning the example of amelioration of the 2nd example of this invention.
[Drawing 9] It is the flow chart which shows the flow of the processing in the semi-conductor manufacturing system of drawing 8 .
[Drawing 10] It is the mimetic diagram showing the semi-conductor manufacturing system concerning the example of amelioration of the 2nd example of this invention.
[Drawing 11] It is the mimetic diagram showing the semi-conductor manufacturing system concerning the example of amelioration of the 2nd example of this invention.
[Drawing 12] It is the mimetic diagram showing the semi-conductor manufacturing system concerning the example of amelioration of the 2nd example of this invention.
[Drawing 13] It is the mimetic diagram showing the semi-conductor manufacturing system concerning the 4th example of this invention.
[Drawing 14] It is the flow chart which shows the flow of the processing in the semi-conductor manufacturing system of this example shown in drawing 13 .
[Drawing 15] It is the cross section showing other examples of the semi-conductor aligner which makes the light source F2 excimer laser concerning this invention.
[Drawing 16] It is the mimetic diagram of the conventional semi-conductor manufacturing system which adopted in-line connection form.
[Drawing 17] It is the flow chart which shows the flow of the processing in the semi-conductor manufacturing system of drawing 16 .
[Drawing 18] It is the conceptual diagram which looked at the production system of a semiconductor device from a certain include angle.
[Drawing 19] It is the conceptual diagram which looked at the production system of a semiconductor device from another include angle.
[Drawing 20] It is the example of a user interface.
[Drawing 21] It is drawing explaining the flow of the manufacture process of a device.
[Drawing 22] It is drawing explaining a wafer process.

[Description of Notations]
1 Reticle Stage
2 Lens-barrel
3 56 Wafer stage
4 Illumination-Light Study System
5 Leading-about Optical System
6 F2 Laser Section
7 Masking Blade
8, 9, 20 Case
10, 11, 12, 21 Air-conditioning machine
13 Reticle Load Lock
14 Wafer Load Lock
15 Reticle Hand,
16, 50, 54 Wafer hand
17 Reticle Alignment Mark
18 Reticle Storage Warehouse
19 55 PURIARAIMENTO section
22,30,35,51 CDS
23, 31, 36, 39, 52 Aligner
24, 30b, 30c, 53 Interface section
25, 26, 32, 33, 37, 38, 40a, 40b In-line port section
28, 29, 57 Manual carrying-in taking-out port section
27 34 Wafer temperature control part
22a, 30a, 35a, 51a Resist spreading section
22b, 22f, 30f, 32a, 33a, 51b, 51f Heating unit
22c, 22g, 30d, 30g, 32b, 51c, 51g Cooling section
22d, 35c, 37a, 38a, 41a, 41b, 51d Heating cooling section
22e, 30e, 35b, 51e Development section
42 Wafer
43 Introductory Tubing
44 Exhaust Pipe
45a, 45b Door
46 Cooling Plate
47 Peltier Device
48 Hot Plate
49 Heater

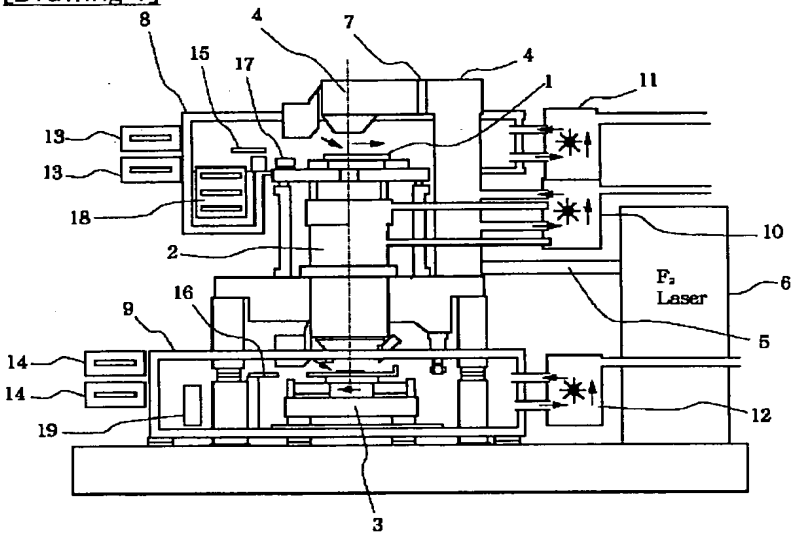
[Translation done.]

* NOTICES *

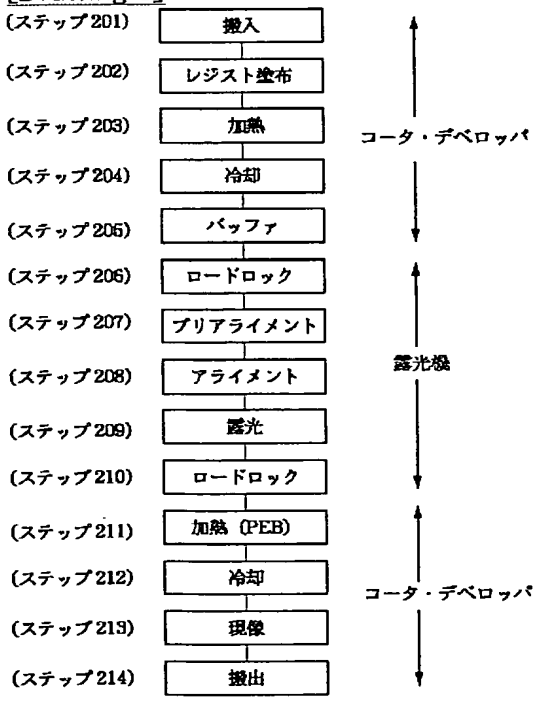
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

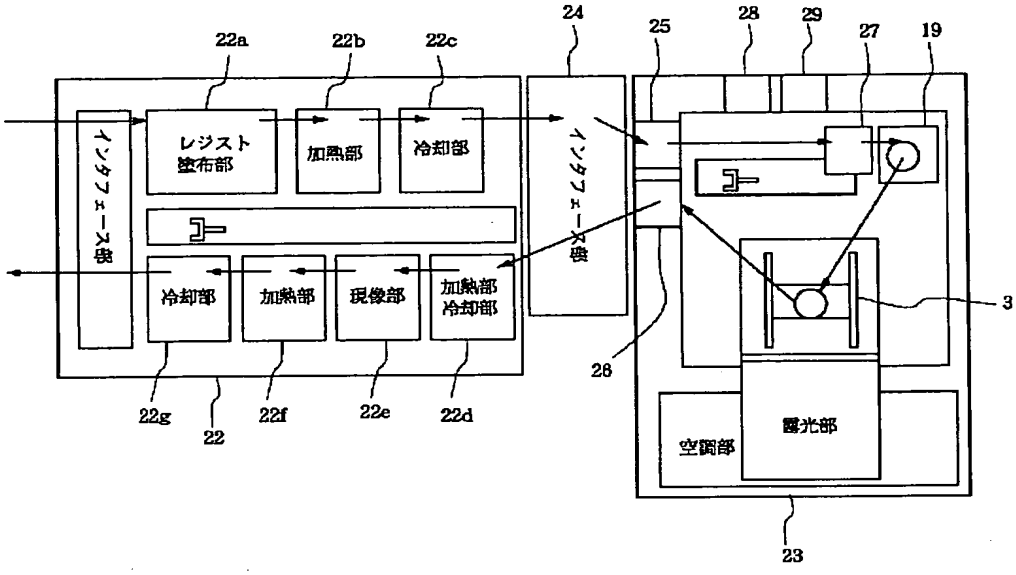
[Drawing 1]



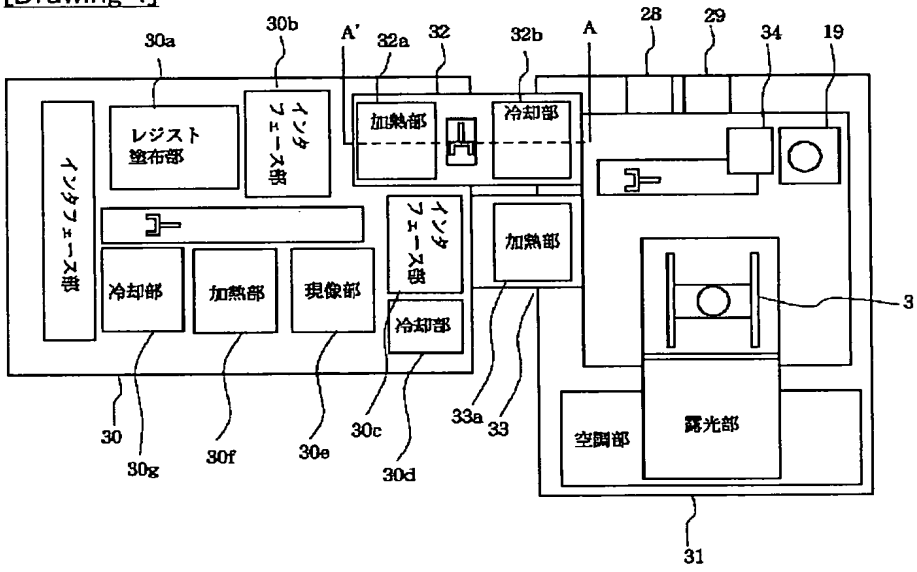
[Drawing 3]



[Drawing 2]



[Drawing 4]



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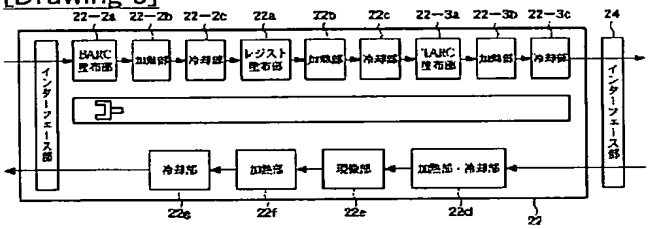
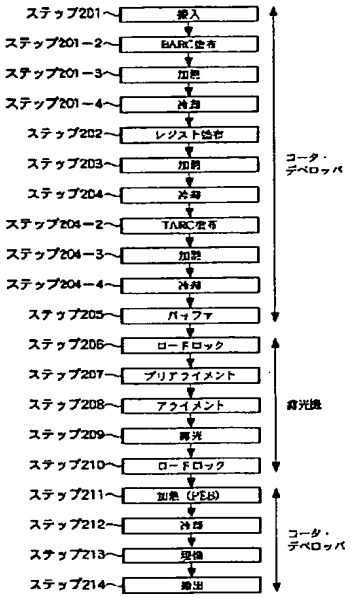


[Drawing 9]



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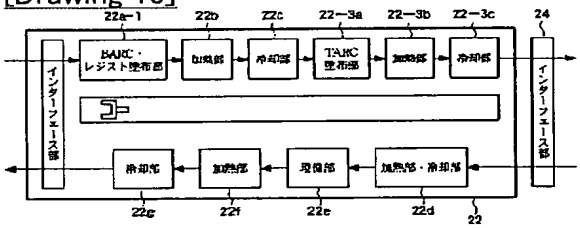

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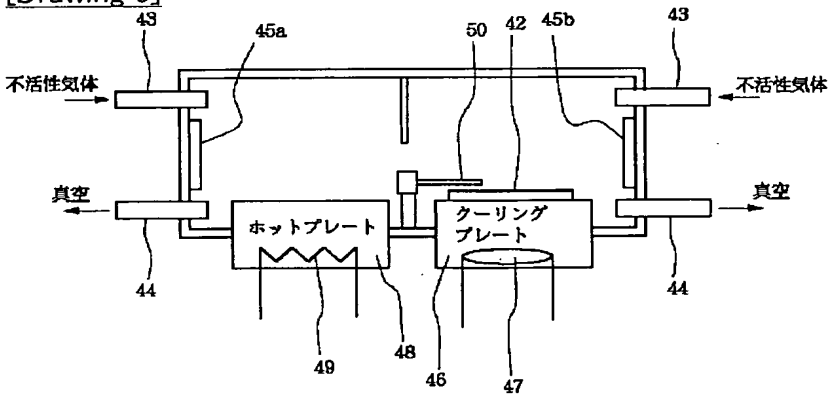

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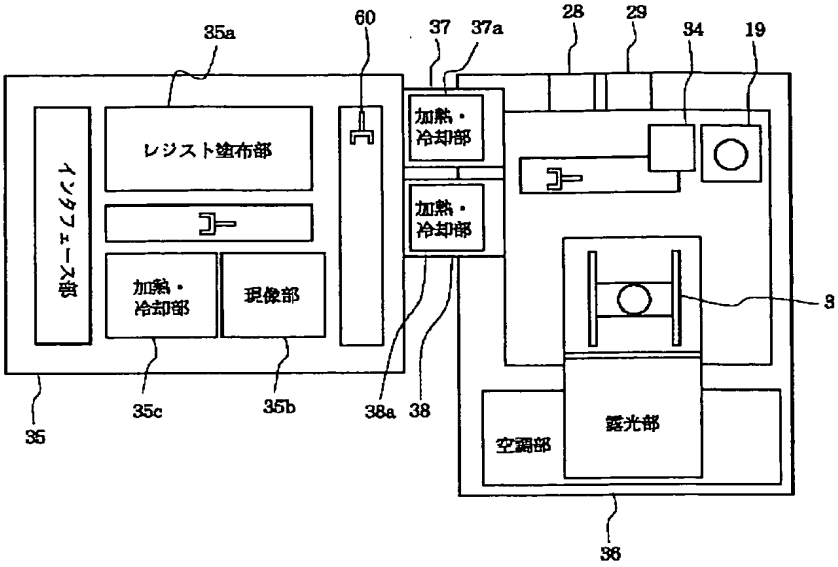
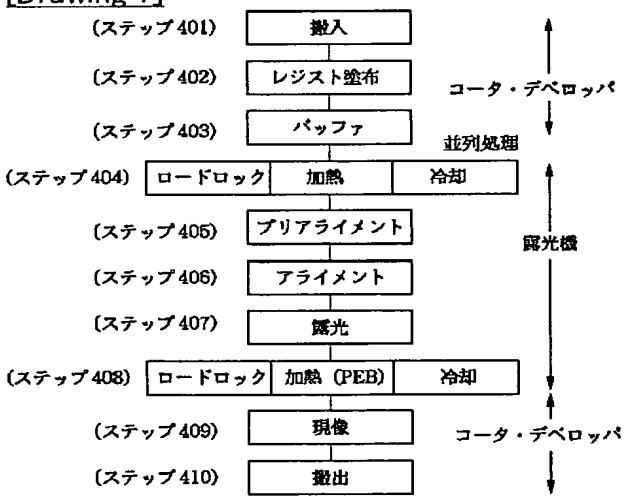
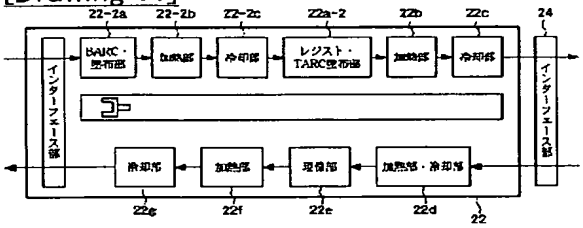


[Drawing 7]



[Drawing 11]



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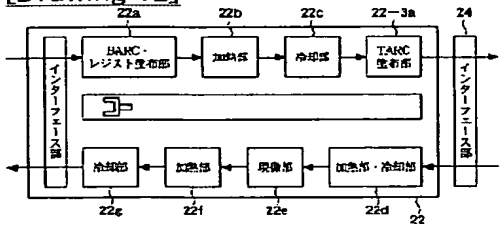

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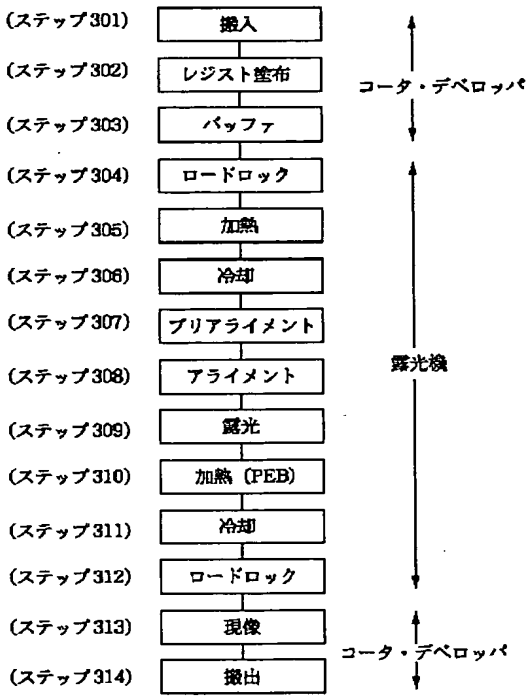
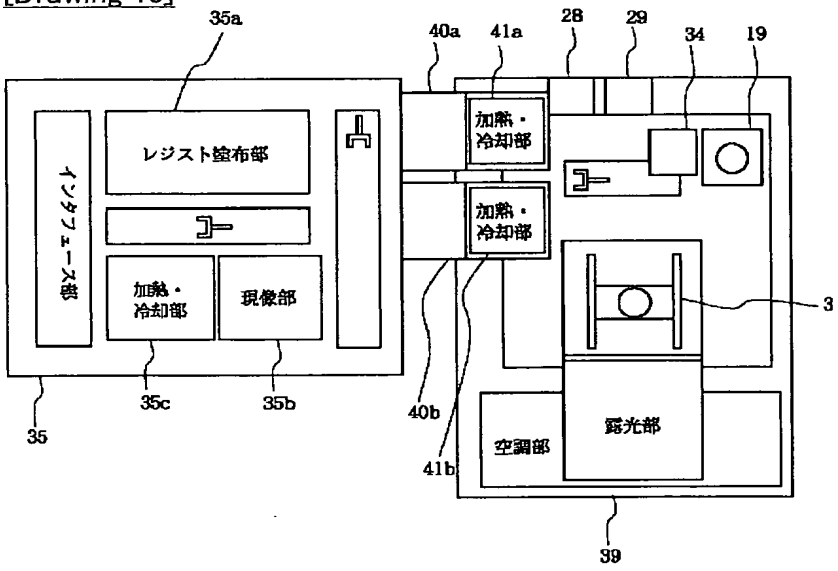


[Drawing 13]



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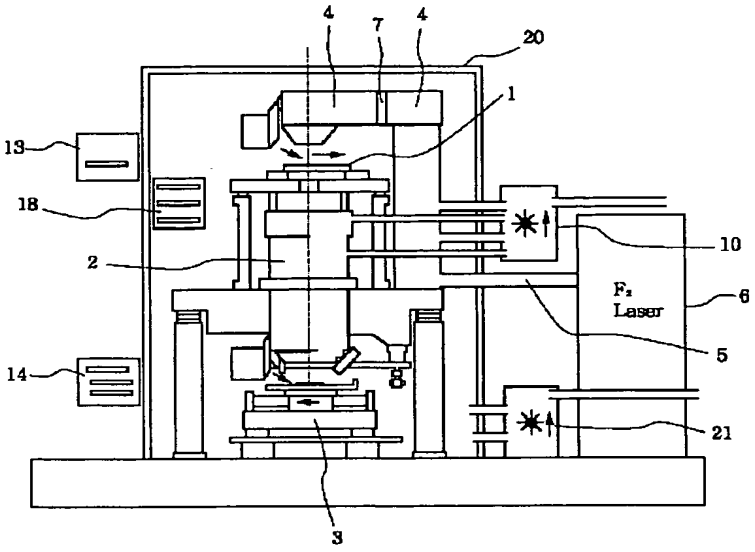
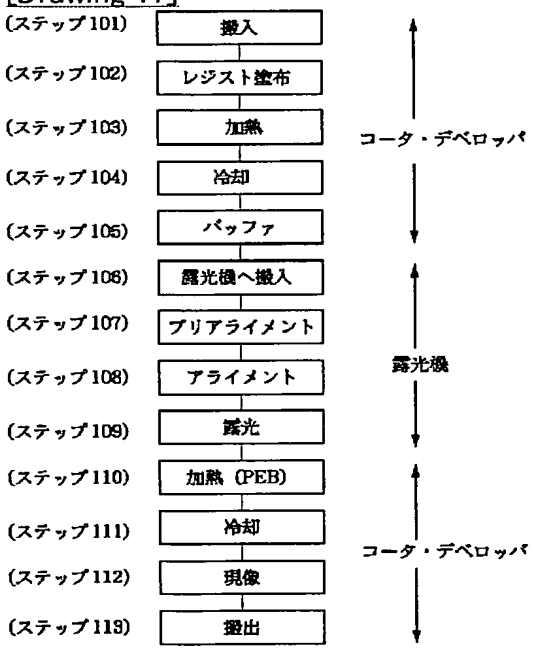


[Drawing 17]



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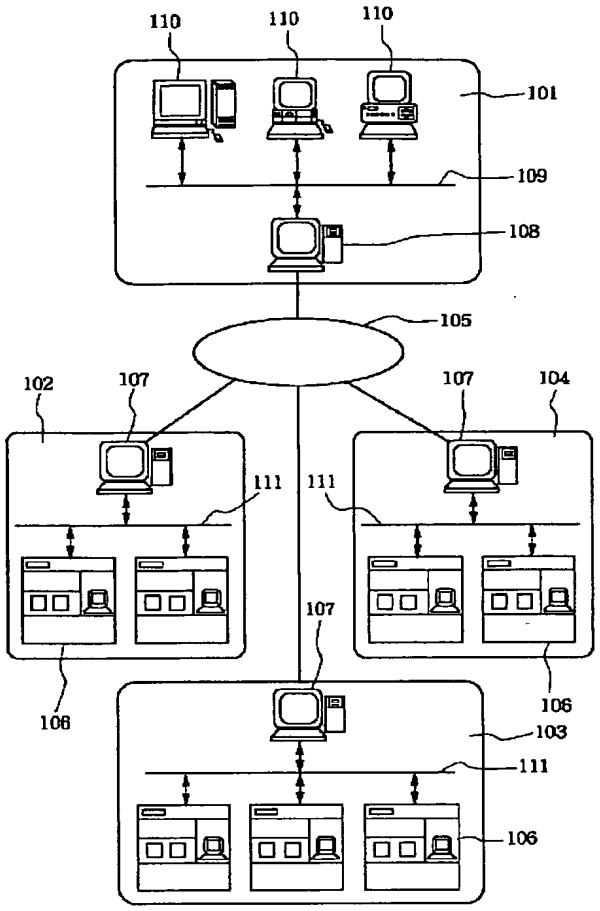

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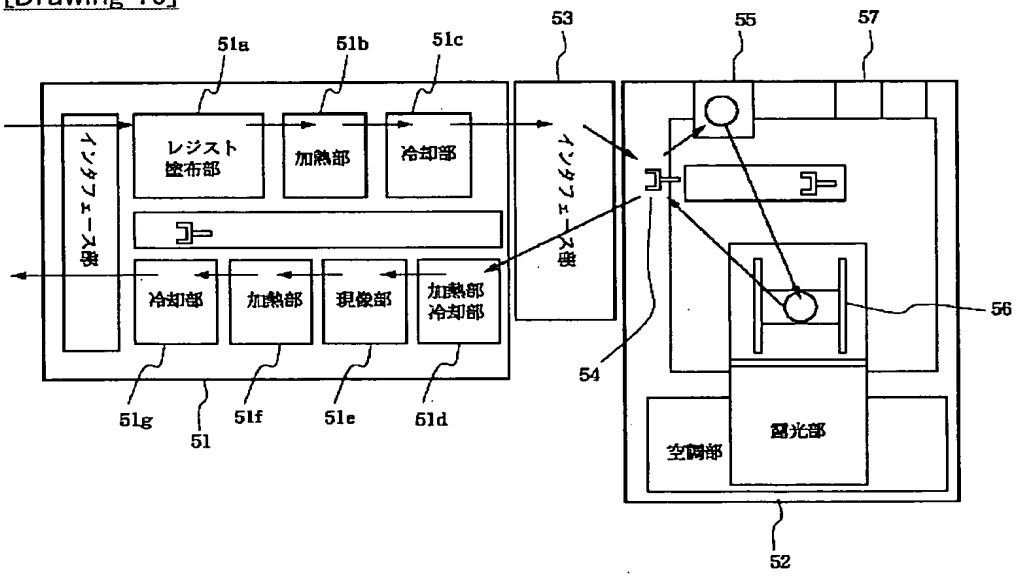

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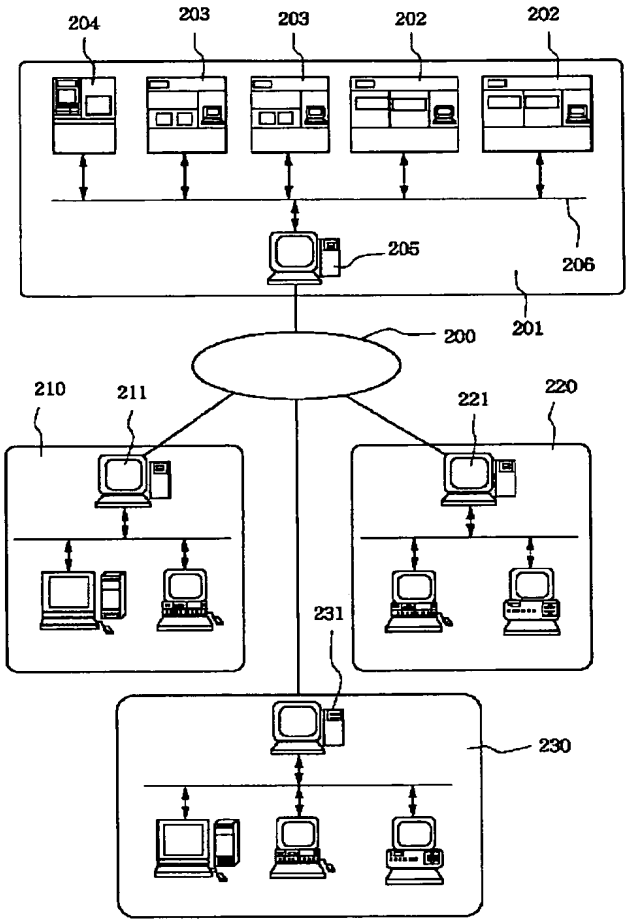

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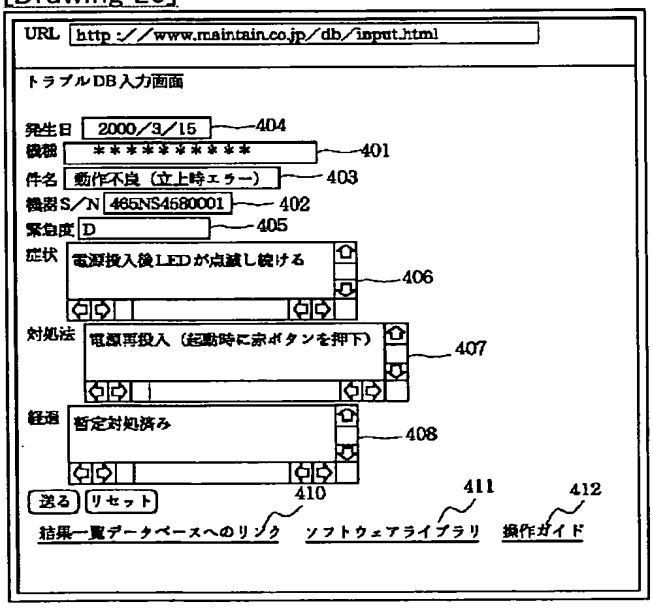
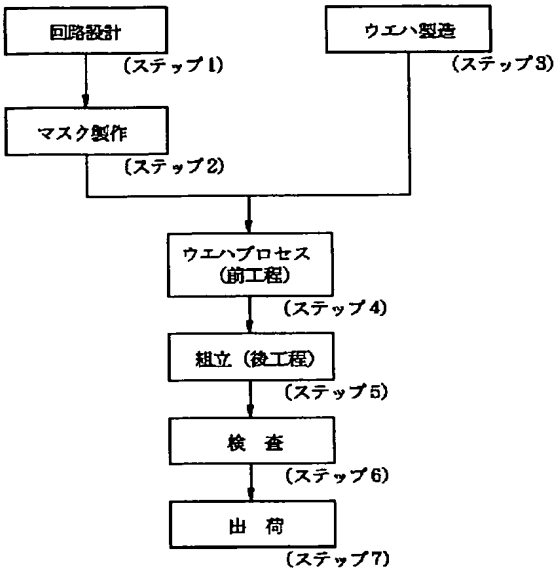
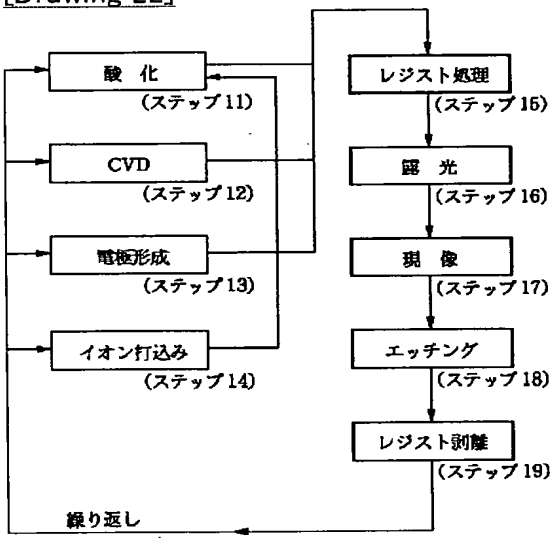


[Drawing 21]



半導体デバイス製造フロー

[Drawing 22]



ウエハプロセス

[Translation done.]